Design of the Readout Electronics for the BGO Calorimeter of DAMPE Mission

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***Abstract*—The DAMPE (DArk Matter Particle Explorer) is a scientific satellite being developed in China, aimed at cosmic ray study, gamma ray astronomy, and searching for the clue of dark matter particles in the near future. The BGO (Bismuth Germanate Oxide) Calorimeter, which consists of 616 PMTs (photomultiplier tubes) and 1848 dynode signals, is a crucial part of the DAMPE payload for measuring the energy of cosmic ray particles, distinguishing interesting particles from background, and providing trigger information. An electronics system, which consists of 16 FEE (Front End Electronics) modules with a total power consumption of about 26 W, has been developed. Its main functions are based on the low power, 32-channel VA160 and VATA160 ASICs (Application Specific Integrated Circuits) for precisely measuring the charge of PMT signals and providing"hit"signals as well. To assure the long-term reliability in harsh space environment, a series of critical issues such as the radiation hardness, thermal design, components and board level quality control, etc., are taken into consideration. Test result showed that the system level ENC (equivalent noise charge) for each channel is about 10 fC in RMS (root mean square), and the timing uncertainty of the hit signals is about 300 ns, both of which satisfy the physics requirements of the detector. Experiments with ^{60}Co radioactive source proved that 20 krad(Si) TID (Total Ionizing Dose) level is achieved, while the heavy ion beam and laser beam tests indicated that its SEL (Single Event Latch-up) and SEU (Single Event Upset) performance in orbit will be acceptable by taking some hardness measures. All the readout modules successfully passed the board-level screening, the sub-system level and finally the satellite system level environmental tests, and behave well in the beam test at CERN (European Organisation for Nuclear Research).**

***Index Terms*—Aerospace electronics, calorimeter, cosmic ray, DAMPE, dark matter.**

I. Introduction

OBSERVING the high energy particles in space is regarded to be a hopeful way for the indirect search for dark matter. Several experiments have already been carried out, such as the ATIC Antarctic Baloon [1], the Fermi/LAT satellite [2], the PAMELA satellite [3] and the AMS02 [4] experiment. In China, a scientific satellite named DAMPE (DArk Matter Particle Explorer) was proposed and approved by the government [5], with a 500 km orbit altitude and a planned mission period of more than 3 years. The major scientific objectives of DAMPE mission are cosmic ray study, gamma ray astronomy, and searching for the clue of dark matter by measuring the spectra of high energy electron/positron and gamma rays.

Fig. 1. Architecture of DAMPE payloads.

As illustrated in Fig. 1, the DAMPE payload consists of four sub-detectors: a Plastic Scintillation Detector (PSD), a Silicon Tracker (STK), a BGO Calorimeter (BGO) and a Neutron Detector (ND). The BGO Calorimeter, which is composed of 308 BGO (Bismuth Germanate Oxide) crystal bars with a size of 2.5 cm $\times$ 2.5 cm $\times$ 60 cm for each, is a crucial sub-detector with the functions of measuring the energy of cosmic ray particles from 5 GeV to 10 TeV, distinguishing positrons/electrons and gamma rays from hadron background, and providing trigger information. All the BGO bars are stacked in 14 layers, with 22 BGO crystals in each layer, as shown in Fig. 2, to achieve nearly 32 radiation lengths. The BGO bars of every two adjacent layers are oriented perpendicularly to provide an X-Y measure of the particle hit position.

II. Requirements from the Detector

According to physics simulation, for a 10 TeV high energy electron, the maximum deposited energy in one bar is about 2 TeV. Meanwhile, the deposited energy from a minimum ionizing particle (MIP) passing through the 2.5 cm thick BGO bar is about 23 MeV. To precisely sample the cosmic ray shower profile, which is regarded to be critical for hadron background rejection, a lower energy limit of less than 0.5 MIP is needed. Therefore a measurement range from 11.5 MeV (0.5 MIP) to

Manuscript received June 16, 2014; revised December 12, 2014; accepted September 08, 2015. Date of publication October 29, 2015; date of current version December 11, 2015. This work was supported by the Strategic Priority Research Program on Space Science of Chinese Academy of Sciences under Grant XDA04040202-4 and the National Basic Research Program (973 Program) of China under Grant 2010CB833002.

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Digital Object Identifier 10.1109/TNS.2015.2479091

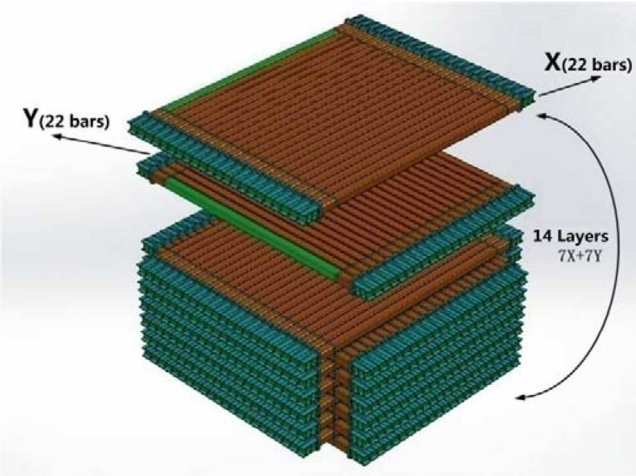

Fig. 2. Arrangement for crystal bars of BGO Calorimeter.

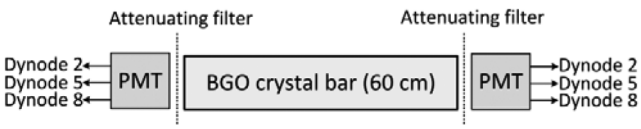

Fig. 3. Readout scheme of BGO detector.

2 TeV, equivalent to about 2×10^5, is required for each BGO bar and exceeds the capability of one single electronics channel, which is typically ensured to be in the order of 10^3.

In order to achieve such large dynamic range, a three-dynode (2, 5 and 8) scheme for the PMT base design is proposed [6][7]. As shown in Fig. 3, each crystal is viewed from both sides by two Hamamatsu R5610A-01 PMTs (photomultiplier tubes). In order to simplify the design of HV (High Voltage) crates, every 11 PMTs of a half layer in one side share the same HV power supply, but the light yields of different BGO bars and the gains of different PMTs can vary significantly. Therefore it is difficult to get a uniform response for the detector units in one layer. An attenuating filter is inserted between each PMT photocathode window and its corresponding BGO bar, to adjust the PMT output response to the deposited energy. Each PMT sends out 3 dynode signals to the readout electronics. Thus there are 1848 readout channels for the 616 PMTs in total.

With proper PMT base design, the relative gain from dynode 2 to 8 is guaranteed to be greater than 10^3 with good linearity, under ordinary high voltage. The basic concept is using uniform readout channels to couple different dynodes, and the relative gains among the three dynodes can be utilized to supplement the dynamic limitation of a single readout channel.

As demonstrated in Fig. 4, the dynode 8, with the highest gain, stands for the low energy range, while dynode 2, with lowest gain, stands for the high energy range, and dynode 5 stands for the medium energy range. Here some assumptions are made: the signal from dynode 8 is adjusted to 100 fC for a single MIP energy deposition; the relative gains from dynode 2 to 5 and from dynode 5 to 8 are both about 30 times; the lower sensitivity limit for the pre-amplifier is less than 50fC and the saturation level is about 12 pC (refer to the VA160 ASIC which will be introduced in the following chapter). Then we can easily conclude that a dynamic range from 0.5 MIP to about 1.1×10^5 MIPs can be achieved.

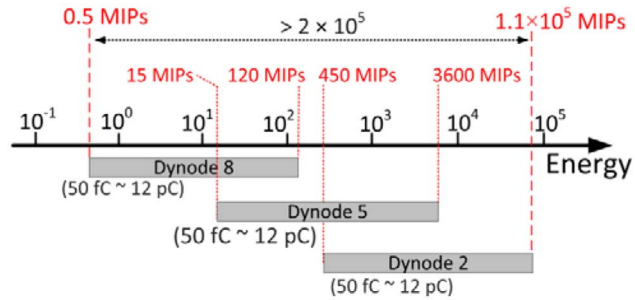

Fig. 4. Design concept to achieve large dynamic range.

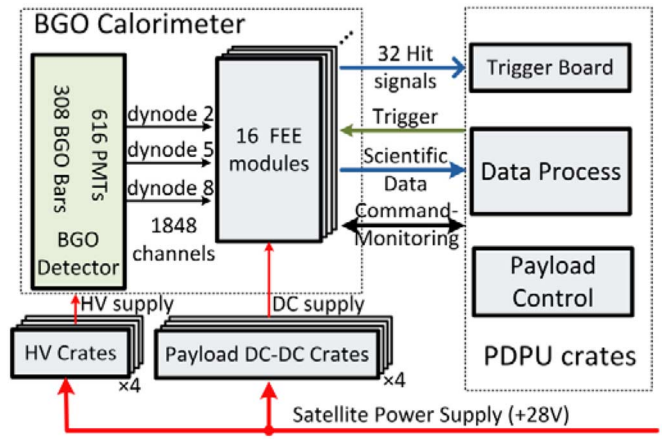

Fig. 5. Architecture of the readout electronics for BGO calorimeter.

Besides performing charge measurement with high precision and large dynamic range, another important function of the BGO calorimeter is providing trigger information for the whole DAMPE payload. According to the physics design scheme, the trigger information is derived from top four layers (Layer 1, 2, 3, 4) and bottom four layers (Layer 11, 12, 13, 14) among the fourteen layers of BGO detector. The signal that carries trigger information is named "hit" signal (also called sub-trigger). If one or more BGO bars in a certain layer are hit by high energy particles, a digital pulse will be generated and sent to the PDPU (Payload Data Process Unit) sub-system. The PDPU receives all the hit signals from corresponding layers, processes them and generates a global trigger signal for the DAMPE payload.

In the BGO detector, only dynode 5 and dynode 8 channels, which stand for low and medial energy range, are used to generate "hit" signals. The trigger threshold in the BGO calorimeter is programmable in orbit, in order to realize flexible trigger logic.

III. System Architecture of the Readout Electronics

The architecture of the readout electronics for BGO calorimeter is presented in Fig. 5. The BGO detector has four vertical sides, each with 154 PMTs and 462 (154×3) signal channels. On each side, there is a group of FEEs taking charge of the readout task for the detector signals.

In addition, there are four HV (High Voltage) crates and four DC-DC crates providing high voltage supply for the PMTs and low voltage supply for the FEEs, respectively. One HV crate and one DC-DC crate are placed on each side, to provide power supply for the nearby PMTs and FEEs.

The FEEs receive the current pulses from PMT dynodes, integrate the charge, and digitize them under the control of trigger signal. The measured result is packed, and transmitted to PDPU by a user-defined serial protocol. The protocol is based on LVDS (Low Voltage Differential Signal) signal level and the clock frequency is 20 MHz.

For the FEEs which read out the top four and bottom four layers of the detector, signals from dynode 5 and dynode 8 will be discriminated to generate the original hit signals. The original hit signal is processed in the FEE to form a RS422 negative pulse with a width of 1000 ns, and sent to PDPU crate.

A Trigger Board in the PDPU crate receives all the hit signals from BGO calorimeter, and determines whether to generate a global trigger signal. The minimum time interval between two adjacent trigger pulses is about 3 ms, thus the signal processing and data transmission process for the readout electronics must be completed within 0.8 ms, to assure that the PDPU has adequate time to pack all the scientific data in a CCSDS 732.0-B-2 [8] format and write them into a nonvolatile mass storage.

The command from PDPU to FEEs and the status information from FEEs to PDPU are both transmitted by a RS422-based 115. 2Kbps half-duplex serial bus (also called command-monitoring bus).

IV. Challenges and Solutions

The large amount of detector components and signal channels, as well as the large dynamic range requirement and the harsh space environment, raise great challenges for the design of the BGO readout electronics.

A. High Integration Level

The first challenge comes from the strict weight and size budget for the satellite, which imposes very stringent constraints on the mechanical design. Thus the effective space for containing the electronics boards is limited as well, resulting in confined area for the PCB (Printed Circuit Board) and cable installation. This leads to a design strategy to reduce the complexity of FEE modules, and to increase the integration level as much as possible.

Fig. 6 illustrates the system configuration for the BGO detector and its readout electronics. Three types of FEE modules are designed, named FEE-A, FEE-B and FEE-C. FEE-A and FEE-B, both receive the 132 input channels in two layers; while FEE-C, with 66 input channels, only readout one single layer. Besides precisely measuring the charge of PMT signals, the FEE-A module (for reading out Layer 1, 2, 3, 4, 11, 12, 13 and 14) needs to provide hit signal to PDPU crate.

In total, there are 16 FEE modules used for the BGO detector, with 4 modules assembled on each side. All the FEE PCB boards are designed within the size of roughly 11 cm $\times$ 38 cm, and installed vertically and very closely to the detector.

B. Low Power Consumption

The second challenge comes from the strict power budget. It becomes a critical issue in the BGO calorimeter not only because of the limited capacity of the satellite's solar battery array, but also resulting from the simplified thermal design mainly due to weight and power reduction strategy. As the FEEs and

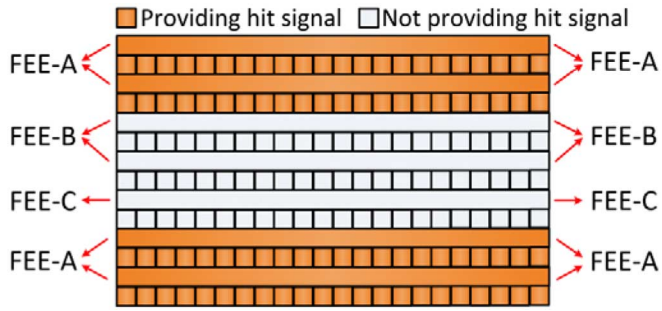

Fig. 6. Configuration for the BGO detector and FEEs.

detector components (PMTs and BGO bars) are assembled together closely, the operating temperature of the detector is directly influenced by the heat produced by the FEEs. Properly reducing the operating temperature is considered to be a useful way to ensure the lifetime of PMTs and to decrease the dark noise. This is significantly achieved by cutting down the power dissipation of FEEs and increasing their thermal conductivity to the outer shielding panel.

Furthermore, as the photon yield of the BGO crystal and the gain of PMT are both proven to have negative temperature coefficients [9], the performance of the BGO detector can also benefit from reducing the power dissipation of FEE boards. Thus all the FEE boards are directly assembled to the outer metal panel, while there are no direct thermal contacts with the inner detector except for the long thin signal cables whose contribution to heat transfer is negligible. All these methods make the temperature field inside the detector more symmetrical and uniform.

Though there are nearly two thousand signal channels needing to be read out, the power budget for all the FEEs is less than 40 W. To overcome this challenge, two types of 32-channel ASIC, named VA160 and VATA160, with the power dissipation of about 150 mW and 180 mW respectively, are chosen as the front end chips to read the signal from PMT, and to provide fast trigger information.

C. Reducing the Crosstalk

The third challenge is the potential crosstalk among the signal channels, due to high density cable assembly and PCB layout, which is further worsen by the large dynamic range of the signals.

For BGO calorimeter, the relative gain from PMT dynode 2 to dynode 8 is greater than 10^3, which makes the crosstalk a severe problem. Even assuming typically very low crosstalk of 0.01%, which can be ignored by most ordinary applications, the maximum crosstalk in BGO calorimeter can reach 10% from dynode 8 to another dynode 2. This suggests that the worst crosstalk is expected to exist between the lowest- (dynode 2) and highest-gain (dynode 8) channels, which may appear like rare high energy events related to the major scientific objective of DAMPE mission.

In order to overcome cross talk, the first step is to use high quality shielded twisted cables to transmit PMT signals, besides careful PMT base PCB layout and bypassing all the dynodes and the anode directly to ground by capacitors [6].

The second step is using different VA160/VATA160 ASIC chips to receive different dynode signals separately. In the FEE

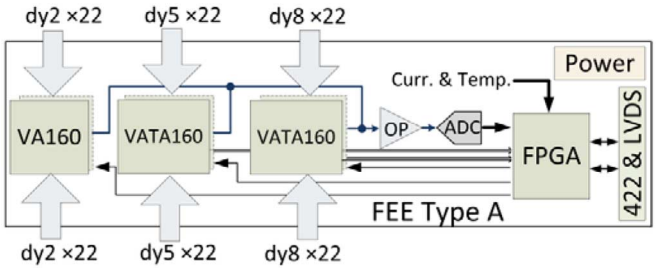

Fig. 7. Block Diagram of FEE-A.

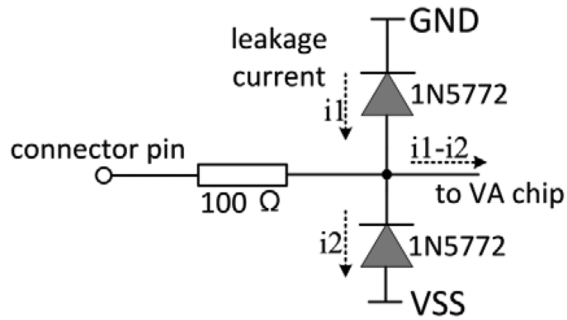

Fig. 8. Block diagram of the protecting circuit.

board, ASIC chips dedicated for dynode 2, 5 and 8 are orderly mounted, with enough distance from one to another. Therefore the dynode 2 chip is the farthest away from dynode 8 chip, so that the crosstalk between them can finally be ignored. These methods, as well as proper PCB layout method, help achieving the large dynamic range of $2*10^5$, which was verified by LED test [6], [7] and CERN beam test in Oct. 2012 [5].

D. High Reliability in Space Environment

There are several other particular requirements derived from harsh space environment, such as good radiation tolerance, proper thermal control, etc.

In order to estimate the performances of the key devices (e.g. the VA160 and VATA160 ASICs and the FPGA chips) in radioactive space environment, both SEE (Single Event Effect) and total ionizing dose (TID) tests were conducted. Several SEU and latch-up protecting methods are adopted, based on the test results.

Meanwhile, thermal simulation for the FEE modules was performed to ensure that all devices will operate in a proper temperature condition.

The methodology of redundant design is adopted in the BGO calorimeter to increase the system reliability. Firstly BGO crystal is viewed on both ends so that the deposited energy in one single bar can be measured by two PMTs together with their corresponding FEEs, which forms a twofold redundancy. In the FEE design it is difficult to use low level redundancy, mainly because of the limited area for PCB layout. But all the power supply cables and all the interface circuits with PDPU are designed with twofold hot redundancy.

The FEE also complies with other regulations for aerospace electronics design, such as ESD (Electro-Static Discharge) protecting, EMC design, Grade 1 derating, etc., to assure the long term reliability.

V. Design of the FEE Module

The BGO calorimeter consists of 8 FEE-A modules, 4 FEE-B modules and 4 FEE-C modules, with 4 modules assembled on each side.

The three types of FEEs are designed with the same scheme, except for that their numbers of input channels are different, and that FEE-A needs to send out hit signals. This paper mainly describes the FEE-A module, which is the most complicated in the three types.

The block diagram of FEE-A is given in Fig. 7. Its major parts will be described below in details.

A. Detector Signal Input and ESD Protecting

In order to avoid the serious crosstalk between large signals (dynode 8) and small signals (dynode 2), cables with shielding layer is a must. Usually a high quality coaxial cable is the best choice, but it is more rigid and the connector occupies too much PCB area, which is not affordable for the FEE design because of the large amount of input channels and limited PCB size.

Finally a kind of space-qualified shielded twisted pair cable and Nicomatic CMM high density connectors are applied. The twisted pair is used as signal and ground (backflow path in fact), and the shielding metal mesh is soldered to ground only on the end of PMT base. Near the FEE board, only the two wires of the twisted pair are inserted into the CMM female connector by a kind of crimp pin, while the male connector is mounted on FEE board directly.

Each connector houses the 22 twisted pairs from the same kind of dynodes from one layer, and feed them to a single ASIC chip. Although there may be tiny crosstalk, with the ratios in the order of 0.1% or less, among adjacent pins in the same connector and chip package, it will not become a severe problem because all these signals belong to the same energy range. Its influence to the final measurement result is negligible, compared to other systematic factors and the electronic noises from the readout ASICs.

An ESD test for VA160 and VATA160 (bonded in a CQFP128 package) conducted in August 2013 indicated that the ESD level of digital IO pins is greater than 2000 V, but the ESD level of analog input pins is just about 500 V, with Human Body Model.

In case of Electro-Static Discharge (ESD) and possible overvoltage "spark" from high voltage components in PMT base, a clamping circuit is designed to protect the front-end ASICs. The diagram is shown in Fig. 8, which is composed of two diodes and a series resistor. A Microsemi silicon diode array (1N5772) with SMT (Surface Mounted Technology) ceramic package is adopted. The ESD protecting level of 1N5772 is 8000 V for contact discharge by the IEC 61000-4-2 standard, according to its datasheets.

But this ESD protecting method may introduce a new problem, which comes from the leakage current from the reverse biased clamping diodes. The leakage are usually dozens of nA at room temperature, and will increase rapidly when the operating temperature rises, obeying the exponential law. This leakage current is not a problem for ordinary digital IOs. However for a charge sensitive amplifier with an internal

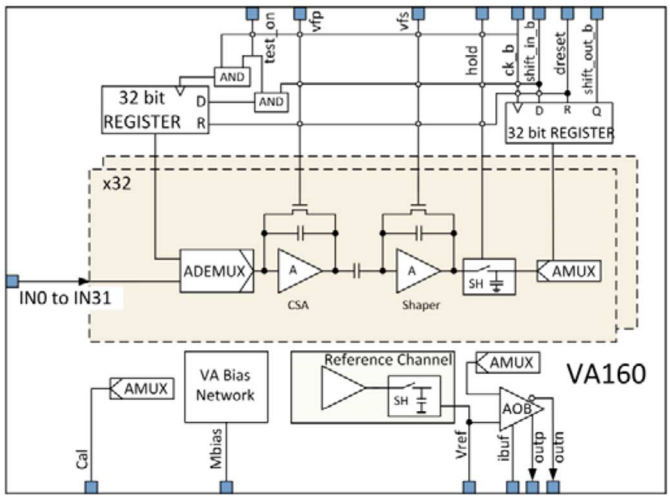

Fig. 9. Block diagram of VA160 ASIC.

feedback resistor with the value of several Mega ohms, it may cause serious interference especially at high temperature.

Fortunately a couple of diodes are usually used at the same time, so that major part of the leakage can flow from one to another directly. As shown in Fig. 8, only the residual (i1-i2) will flow to the VA chip.

In order to reduce the influence of this residual current, firstly a strict screening process was conducted for every 1N5772 components, at room temperature (for the qualification model) and 55°C (for the flight model). Only the chips having low leakage currents (e.g. less than 60nA) and best symmetry for each diode pairs were selected for board assembly. Secondly all the FEE boards were tested at 55°C, and a very few of 1N5772 components who affected the FEE performance were replaced.

B. Charge Measurement

The charge measurement function is performed by VA160 and VATA160 ASICs. There are 2 VA160 and 4 VATA160 used in an FEE-A module, 6 VA160 used in an FEE-B module and 3 VA160 used in an FEE-C module.

VA160 and VATA160 ASICs, optimized for the PMT dynode signals of DAMPE (for Plastic Scintillation Detector and BGO detector), are both developed by IDE AS Inc. in Norway [10]. The VA160, which can be seen as an advanced version of the VA32HDR14.2 ASIC, has 32 analogue input channels for measuring the charge of PMT dynode signals, with a dynamic range from −3 pC to 12pC and an INL error less than 2%.

The VATA160 can be seen as a combination of one VA part and one TA part. The VA part is exactly the same as VA160; while the TA part is an advanced version of TA32CG ASIC and is designed to generate fast trigger ("hit" signals for BGO detector).

The block diagram of VA160 is illustrated in Fig. 9. Each input channel is composed of a charge sensitive pre-amplifier (CSA), a CR-RC shaping amplifier and a sample-hold circuit (SH). Signal from PMT dynode is integrated by CSA and then shaped into a semi-Gaussian pulse with the peaking time of about 1.8 us, while the signal peak is proportional to the input charge.

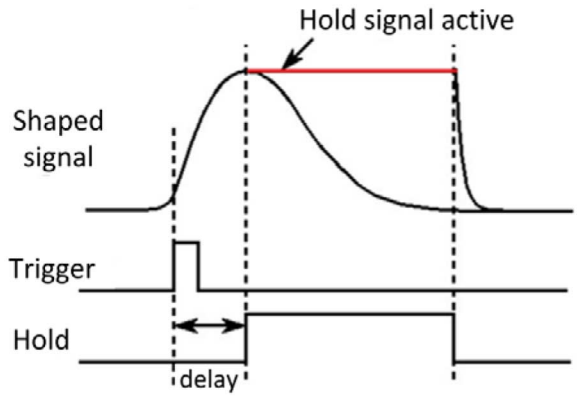

Fig. 10. Time diagram of charge measurement process with VA160.

As shown in Fig. 10, a hold signal is used to sample all the analog channels at the same time. When Hold goes high, the analog switches in all the sample-hold circuits will be turned off, and the 32 shaping amplifier outputs are stored in their capacitors and wait for being sent out sequentially in differential current, under the control of a shifter registers chain and an analog multiplexer. Besides the 32 input channels, there is a dummy channel inside the ASICs, which is used as a reference for the output driver, to subtract the common noise and to compensate the temperature drifts.

The output current drivers of all VA160 and VATA160 chips in one FEE are wired together and led to a current-to-voltage conversion circuit formed by operational amplifiers with the output range from about 0 to 5 V, and digitized by an AD976A chip, which is a 16-bit ADC with an input range from −10 V to +10 V but only need single +5 V supply.

Both theoretical analysis and test results suggest that there is an obvious negative correlation between the noise and the output impedance of the detector. As the parasitic capacitance of signal cables are fixed (mainly depending on the cable parameters and length), the only practical treatment is to constrain the output capacitance and resistance of PMT base. The value for all components in PMT base are carefully evaluated and verified by test results, and finally a 10 k ohm output series resistor and a 1 nF output series capacitor are chosen.

The delay time of Hold signal is another critical issue for the measurement error. A test result is illustrated in Fig. 11, in which the relation between the measured charge (in ADC code) and Hold delay are shown. The curves just seem like top part of a CR-RC semi-Gaussian waveform and the peak region is relatively smooth. We can see that a jitter of +/−150 ns around "hold" delay value corresponding to the maximum may cause a variation of less than 2% in the conversion.

In FEE module, the Hold signal is derived from the system Trigger, and the delay time can be configured in orbit, in order to catch the peak of shaper output in different trigger modes.

C. Hit Signal Generation

The FEE-A module needs to send out hit signals and this function is performed by VATA160 ASIC.

The block diagram of VATA160 is shown in Fig. 12.

The VATA160 is composed of VA part and TA part. There are 32 channels in the TA part as well. Each channel contains

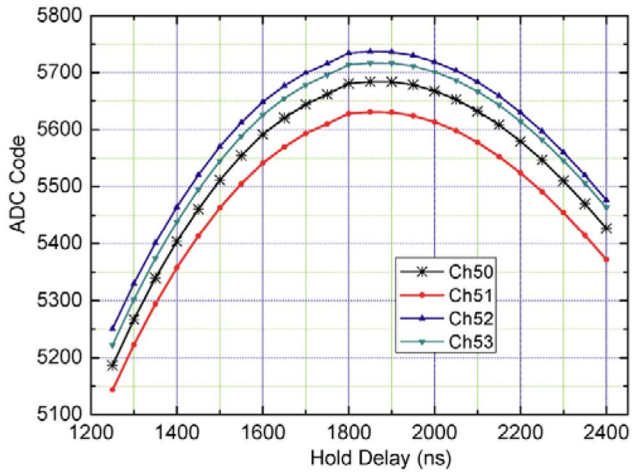

Fig. 11. Measurement result (ADC code) versus Hold delay.

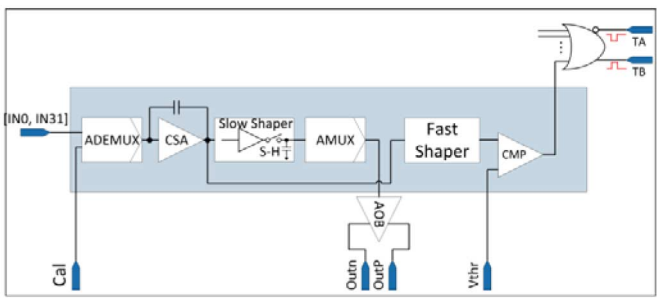

Fig. 12. Block diagram of VATA160 ASIC.

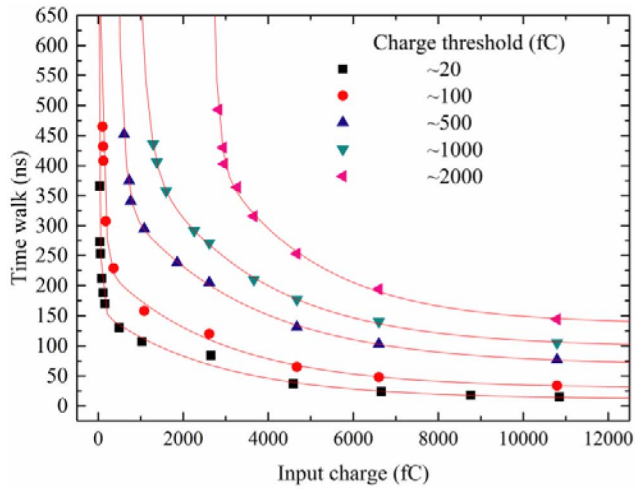

Fig. 13. Time walk versus input charge, for different thresholds.

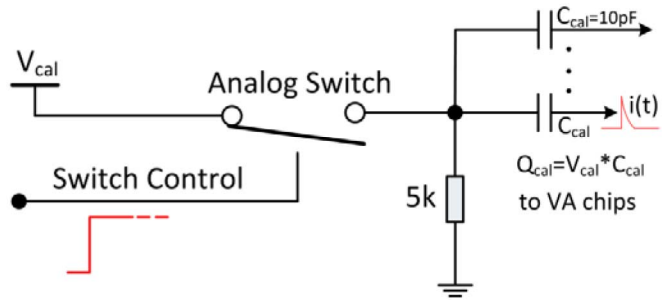

Fig. 14. Block diagram of the calibration circuit.

a faster shaper and a comparator. The integrated pulse from the CSA (of VA part) will firstly be shaped into a fast narrow pulse and then discriminated by a comparator, to generate a digital signal. All the 32 outputs of TA part are internally OR'ed together, thus the output signal (in the form of differential current, named TA and TB) is shared by all input channels, which greatly simplifies the system design.

Each FEE-A is in charge of two BGO layers, while each layer needs two hit channels: the dynode 5 hit and dynode 8 hit. Therefore 4 VATA160 chips are employed in one FEE.

On one hand, the signal from BGO detector is not fast, because of the 300 ns fluorescence decay time of BGO crystal. On the other hand, due to the parameter dispersion of BGO crystals and PMTs, it's difficult to make the detector units on the same layer have a uniform response to the energy deposition. Thus an important issue for VATA160 is the time walk of hit signals, which may cause error for charge measurement, as indicated in Fig. 11.

A detailed test was conducted [11], using an LED source to illuminate the PMT. The LED is driven by a BGO-liked current pulse (an exponential curve with a 300 ns decay time). The test result is shown in Fig. 13, which gives the relationship between time walk and input charge at different thresholds. From the figure we can draw a conclusion that a lower threshold-to-signal ratio leads to smaller time walk error. For a threshold-to-signal ratio less than 1/2, the time walk is about 300 ns (can also be seen as $+/-150$ ns), which is acceptable for the experiment.

Another important solution is to control the uniformity of the detector units in the same layer during component test and assembly procedures. It is beneficial from both reducing time walk and improving the trigger efficiency. Finally a less than 20% uniformity deviation (in sigma) in each layer was achieved, for both the qualification model and the flight model.

D. Calibration Circuits

In order to monitor the performances of electronics in orbit, a calibration circuit is designed, utilizing the calibration function of VA160 and VATA160 ASICs. This calibration circuit is also used to test the hit generation function of VATA160.

As shown in Fig. 14, the calibration circuit is mainly composed of an analog switch and a 5 k ohm resistor. When the analog switch is turned on, the circuit will generate a step pulse (from 0 to V_{cal}), and a current pulse is injected into the ASIC chip through an external 10 pF capacitor (C_{cal}).

A DAC and an op-amplifier are used to provide the calibration voltage (V_{cal}), and the calibration charge injected to each VA chip is the product of V_{cal} and C_{cal}. In the VA ASIC, an analog de-multiplexer is used to determine which input channel is enabled for calibration. By sequentially select the input channels and gradually sweeping the calibration voltage, the scan curve of all channels in a FEE can be obtained. One calibration curve is illustrated in Fig. 15, in which the nonlinearity from 0 to 13 pC is less than 1% and much better than the design specification (2%).

E. Monitoring Circuits

Each FEE module has 2 current monitoring channels, for the positive (+2.5 V) and negative (−2.5 V) supply current

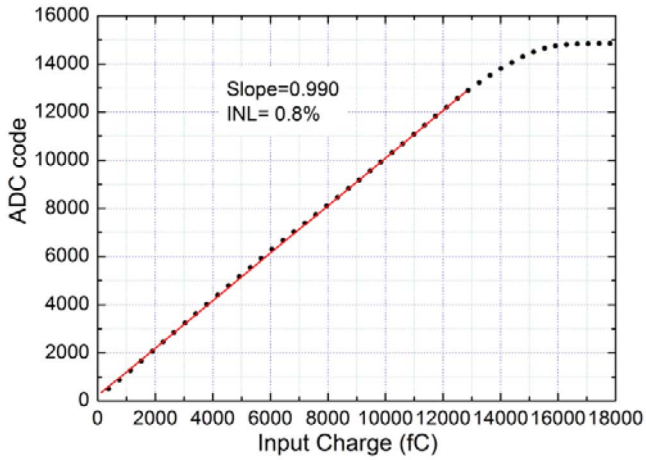

Fig. 15. Calibration scan curve of a FEE input channel. The offset (also called pedestal) values of all FEE channels are around zero, within a maximum range of -300 to 300 ADC bins.

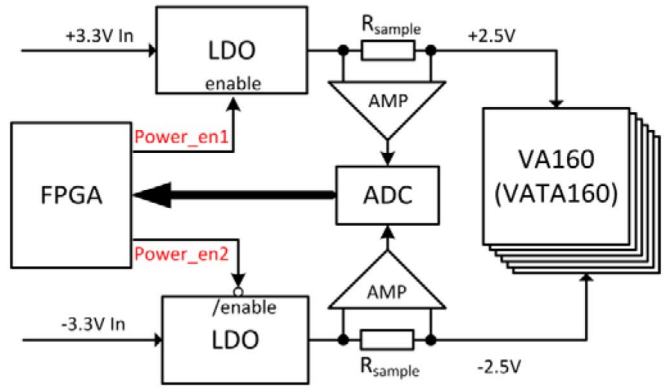

Fig. 16. Block diagram of SEL protecting solution.

of all VA160/VATA160 chips, respectively. The current monitoring circuits are composed of resistors (1/4 ohm), op-amplifiers, and a multi-channel ADC shared with the thermal monitoring circuit.

Four thermal resistors are used for each FEE, among which three are used to obtain the temperature of BGO crystals and the other one is used to obtain the temperature of one of the VA160/VATA160 packages.

In addition to the current and temperature monitoring functions, the values of 32 status registers (32 bytes in total) in the FPGA logic are sent to PDPU as well. PDPU will inquiry temperature information and FPGA status every 16 seconds, and inquiry current information every second.

F. Radiation Protecting

Three kinds of radiation effects are taken into consideration for the FEE design, including the TID (Total Dose) effect, the SEU (Single Event Upset) effect and the SEL (Single Event Latch-up) effect.

The DAMPE satellite will operate in a near earth orbit with the height of 500 km. According to simulation, with 3 mm aluminum shielding, the total dose during three year is less than 3 krad. To ensure an adequate RDM (Radiation Design Margin), the design specification for BGO electronics is 20 krad, which can be achieved by most of the ordinary components.

For the BGO FEE modules, the detector with a weight of about 800 kg (mainly contributed by BGO crystals) is an ideal shielding for about 2π solid angle. The other 2π solid angle is mainly shielded by the BGO envelope panels, the crates of other sub-systems and the satellite supporting structures, with a total thickness of at least 3.6 mm in aluminum, which can provide a good condition for TID protection.

Several total dose tests were carried out in the end of 2013 to study the TID tolerance of VA160 and VATA160 ASICs, using ^{60}Co gamma sources with an activity order of about 10^4 Curie. Test results showed that the electric performances and the supply currents of both ASICs remain rather stable, with the total dose greater than 30 k rad and a dose rate of about 5 rad/s.

The SEU protection is also taken into account for sequential logic and memories. Firstly TMR (Triple Modular Redundancy) method is used for the 165 bit configuration registers of VATA160, by IDE AS. For the FEE design, the APA600 and APA300 FPGAs, from Actel flash-based ProASIC Plus (APA) family, are chosen to implement the control logic of FEE.

The APA FPGA uses the floating gate to store the configuration information of the logic elements, which is regarded to be immune to SEU. Several heavy ion beam tests from 2012 to 2013 were performed, and the test results proved that the APA300 and APA600 is SEL immune and the floating gate is also stable.

However, the registers and memories in logic tiles and RAM blocks are still SEU sensitive, just like other SRAM-based FPGAs. In order to overcome this problem, several design methodologies were adopted, such as TMR and CRC (Cyclic Redundancy Check), etc., whose effectiveness have already been verified by heavy ion beam tests [12].

Heavy ion beam tests showed that VA160 and VATA160 are sensitive to SEL, with the threshold of about 21 MeV$*$ cm^2/ mg and 11 MeV$*$ cm^2/ mg, respectively. By using the CREAM96 program, the SEL rates are calculated to be $2.7\mathrm{E}-5\mathrm{device}^{-1}*\mathrm{day}^{-1}$ for VA160 and $8.1\mathrm{E}-5\mathrm{device}^{-1}*\mathrm{day}^{-1}$ for VATA160, which cannot be neglected.

A protecting solution is proposed and its principle is shown in Fig. 16. The supply current of VA160/VATA160 ASICs are sampled by the monitoring circuit, in a period of 100 us. If the currents exceed the preset threshold, the FPGA will send control signals to the two regulators (LDO) immediately, to cut off the power supply of VA160/TA160. About 30 ms later, when the SEL disappears, the FPGA enables the power supply again. A laser-pulse experiment, in which infrared laser-pulse is used to induce latch-up events in the ASICs, is performed to verify this solution. Test results showed that every SEL events can be detected quickly and successfully recovered, and there is no performance degrading observed even after more than 8000 times of latch-up.

VI. Mass Production and Integration Tests

The qualification model of the BGO calorimeter was assembled at the end of 2013, and the flight model was assembled in early 2015. For each model, twenty BGO FEE modules, including four spare ones, were mass-produced in a factory, complying with aerospace quality control regulations. All the modules were tested with a strict procedure, and passed the screening

Fig. 17. Photograph of the QM FEE board (Type A).

Fig. 18. Photograph of the BGO calorimeter qualification model after assembly.

procedure with 16.5 cycles from $-45°$ C to $75°$ C under ordinary pressure.

Fig. 17 is the photograph of an FEE-A module. Three ASICs are mounted on top side while the other three ones are mounted on bottom side. PMT signals from dynode 2, 5 and 8 are sent to the three ASIC (top or bottom side) from left to right respectively. FEE-B possesses six VA160, with three chips on each side, while FEE-C only has three VA160 on top side. According to the test result, the total power consumption for the 16 FEEs is 26 W, which is much better than the budget.

After 16 FEE modules being installed with the BGO detector, a series of sub-system level environmental tests were conducted for both the qualification model (as shown in Fig. 18) and flight model, including the EMC (Electromagnetic Compatibility) test, the vibration test, the thermal cycling test, thermal-vacuum test, and a 360-hour burn-in test just for the flight model. Later a series of system-level integration tests were carried out, and the BGO Calorimeter was indicated to be compatible with other sub-systems of the satellite, and both FEE boards and PMTs can operate well in the desired temperature range in space. The test result also demonstrated that the system-level equivalent noise charge for each FEE channel is about 10 fC in RMS, which is much less than 0.5 MIP signal (50 fC) and meets the design specification.

From late October to mid-November in 2014, two beam tests were conducted for the qualification model, with the PS (Proton Synchrotron) and SPS (Super Proton Synchrotron) facilities at CERN, using low energy (0.5 $\sim$ 5 GeV) and relatively high energy (5 $\sim$ 250 GeV) particles respectively. The test results successfully verified the design concepts and performance of the BGO Calorimeter, and also showed that the readout electronics is properly designed and fully functional.

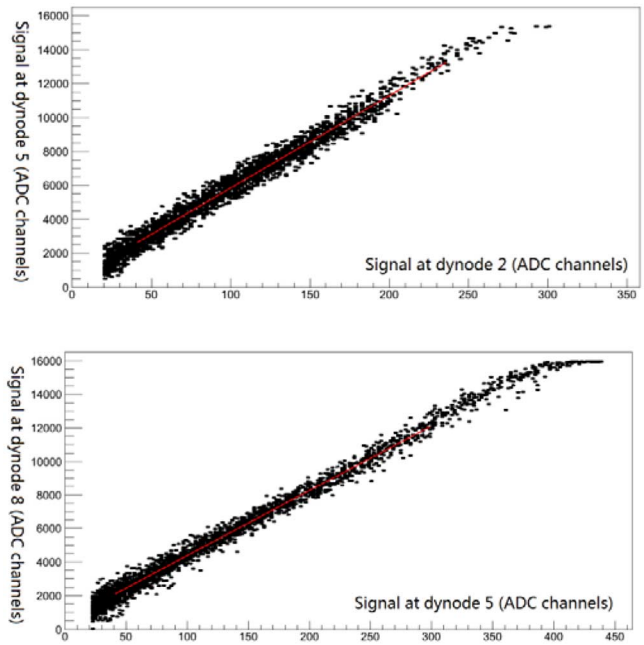

Fig. 19. Top: Correlation between dynode 2 and dynode 5 signals from one PMT; Bottom: Correlation between dynode 5 and dynode 8 signals from the same PMT. The data samples are acquired from one run at SPS using 250 GeV electrons.

Fig. 19 demonstrates the correlations among the signals from dynode 2, dynode 5 and dynode 8 of one PMT unit. The linearity and relative-gain (greater than 30) are both satisfied. The crosstalk appears not affecting the linear relation among different signals, because good linearity and reasonable gain value can be seen between the three dynodes.

VII. Summary

A high integration level, low power and large dynamic range readout system has been successfully designed and produced, for the BGO Calorimeter of DAMPE satellite. It consists of 16 FEE (Front End Electronics) modules and 1848 signal channels, with a total power consumption of only 26 W, and has a large dynamic range of 2×10^5 for the detector unit.

Several special issues regarding the space-craft engineering were taken into account, such as thermal design, radiation tolerance, quality control, etc. The total dose level is proven to be greater than 20 krad(Si), and the influence of in-orbit SEL and SEU are minimized to negligible levels by adopting effective hardening methods. The BGO Calorimeter, including its electronics boards, has successfully passed a series of environmental tests and operated compatibly with other sub-systems during the satellite level integration tests.

At the end of year 2014, two beam tests were successfully conducted at CERN with PS and SPS facilities. The test results showed that the performances of BGO Calorimeter, such as the energy linearity and resolution, are consistent with expectations, indicating that the electronics design satisfies the physics requirements as well.

Acknowledgment

We would like to thank to Dr. Jianhua Guo, Mr Yiming Hu, Mr Dengyi Chen, Dr. Fei Zhang and Dr. Jie Kong for helpful

discussions and useful suggestions. We also would like to thank all the people from DAMPE collaboration who helped make this work possible. This work was supported in part by the CAS Center for Excellence in Particle Physics (CCEPP).

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